~~significant bits~~ within a predetermined number of the most significant bits of an instruction word.

37. (Previously presented) The method of Claim 36, wherein the act of providing a compressed instruction set further comprises encoding a plurality of said compressed instructions with source register fields located in a predetermined relationship to one another.

38. (Previously presented) The method of Claim 37, wherein the act of encoding with said predetermined relationship comprises encoding the source register fields for respective ones of said plurality of compressed instructions at identical locations.

39. (Previously presented) The method of Claim 35, wherein the act of providing a compressed instruction set comprises encoding all of the immediate data fields such that they start from the least significant bit (LSB).

ok to enter correction. MS. 6-21-2005 per Robert Boyd, under Reg No 39,990

40. ~~(Previously presented)~~ (Currently Amended) A method of operating an extended pipelined digital RISC processor having an instruction pipeline comprising at least instruction fetch, decode, and execute stages, a storage device configured to hold a plurality of program instructions, and an optimized instruction set comprising both 16-bit and 32-bit instructions, the method comprising:

providing an extension instruction set having a plurality of user-selected extension instructions;

providing a compressed instruction set derived at least in part from said extension instruction set;

encoding a plurality of compressed instructions from said compressed instruction set into an instruction word having an op-code;

assigning one of a plurality of predetermined values to at least one bit within a status register within said processor; and

executing at least one of said compressed instructions from said instruction word within said pipeline based on a second predetermined value present in said status register.

41. (Previously presented) The method of Claim 40, wherein said act of encoding comprises encoding two 14-bit compressed instructions into a 32-bit aligned